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EXAMINER	
KENNEDY, JENNIFER M	
ART UNIT	PAPER NUMBER
2812	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/908,941	HIRASE ET AL.	
	Examiner	Art Unit	
	Jennifer M. Kennedy	2812	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 March 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) *1 and 2* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *3-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *12/14/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

In view of Applicant's arguments and the amendment to the claims, the rejections of claims 3 and 9 under 35 U.S.C. 112 second paragraph, as being indefinite, are withdrawn.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 12, 14, 16, and 18 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. The limitation of patterning a conductive film on the semiconductor substrate, wherein the height of the step at the time of removing the film is adjusted to a predetermined height that is equal to a depth etched during said patterning of the conductive film is not supported by the specification. The examiner notes that Applicant has taught in paragraph 76 that the "height of each step is substantially equal to the depth of the insulation 41a that is

etched in subsequent processes, but this does not provide support for the limitations of claims 12, 14, 16, and 18.

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> **The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.**

Claims 12, 14, 16, and 18 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Claims 12, 14, 16, and 18 require patterning a conductive film on the semiconductor substrate, wherein the height of the step at the time of removing the film is adjusted to a predetermined height that is equal to a depth etched during said patterning of the conductive film is not supported by the specification. While it is understood from the specification that the "height of each step is substantially equal to the depth of the insulation 41a that is etched in subsequent processes it is not understood how the height of the step at the time of removing the film is adjusted to a predetermined height that is equal to a depth etched during said patterning of the conductive film. The examiner believes the claim is stating that the step created by removing the silicon nitride, and therefore equal to the thickness of the nitride, is adjusted to be equal to the depth etched during said patterning of the conductive film. First, it is not understood what the depth is when patterning the conductive film. Instead, is Applicant intending on reciting that the insulation film, 60, is patterned and the depth from the top of the insulation to the substrate is the same depth as the top of the insulation to the top of the step? In Applicant's Figure 2 it is noted that

the step no longer exists. Second, as claimed, if the step no longer exists then the depth etched during said patterning of the conductive film is nothing. The examiner requests clarification.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 3-4, 7-10,and 11-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kuroi et al. (U.S. Patent No. 5,889,335) and Zhang et al. (U.S. Patent No. 6,303,458) in view of Krivokapic et al. (U.S. Patent No. 6,087,208).

In re claim 3, Kuroi et al. disclose the method of making a semiconductor device comprising:

forming a film on an upper surface of a semiconductor substrate (3, 4);

forming an element partitioning trench (10C) and a mask aligning trench (10A) in a semiconductor substrate (1);

simultaneously depositing an insulation (2) in the element partitioning trench and the mask aligning trench by a CVD process, wherein no other insulation layer has been deposited by a plasma process in the trenches prior to the insulation being deposited;

applying a protective mask (51) on the insulation deposited in the element partitioning trench to fully cover the element partitioning trench (see Figure 4);

etching the insulation deposited in the mask aligning trench to remove some of the insulation while the insulation deposited in the element partitioning trench is covered by the protective mask (see Figure 4 and column 14, lines 37-41);

removing the protective mask (51, see Figure 5, and column 14, lines 49-51); and

flattening an upper surface of the semiconductor device (see column 14, lines 42-54) and selectively removing the film so that a step is formed between the upper surface of the semiconductor substrate and an upper surface of the insulation deposited in the element partitioning trench (see column 14, lines 49-63 and Figure 5). The examiner notes that the insulation is made planar with the silicon nitride film, and then the silicon nitride film and the silicon oxide film are removed, thus a step will be formed between the upper surface of the substrate and the upper surface of the insulation layer as shown in Figure 5 of Kuroi et al. Further, the examiner notes that Applicants' own admitted prior art discloses that a step will be formed in this manner (see specification, page 3, line 25 through page 4, line 30, and Figure 1f).

Kuroi et al. does not disclose the method of removing the insulation deposited in the mask aligning trench has an upper surface located lower than the upper surface of the semiconductor substrate.

Zhang et al. discloses the method wherein the removing the insulation deposited in the mask aligning trench has an upper surface located lower than the upper surface of the semiconductor substrate (see Figure 4B and column 2, lines 35-50). It would have been obvious to one of ordinary skill in the art at the time the invention was made

to remove the insulation deposited in the mask aligning trench has an upper surface located lower than the upper surface of the semiconductor substrate, because as Zhang et al. disclose the method ensures that the step distance is great enough for the alignment mark to be readable (see Zhang et al. column 2, lines 35-50).

Kuroi et al. does not disclose the method of depositing the insulation by performing a chemical vapor deposition process consisting of high density plasma chemical vapor deposition (HDPCVD). Krivokapic et al. discloses the method of forming an insulation layer (34) by a chemical vapor deposition process consisting of HDPCVD (see column 5, lines 49-65). It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the insulation layer of Kuroi et al. by the HDPCVD process of Krivokapic et al., since as Krivokapic et al. disclose, HPCVD is a self-planarizing process which allows for a reduction of CMP times required in the subsequent steps.

In re claim 4, Kuroi et al. also disclose the method of forming a coating (4) on the semiconductor substrate, wherein the coating has a pattern of openings corresponding to the element partitioning trench and the mask aligning trench and etching the semiconductor substrate using the coating as a mask to form the element partitioning trench and the mask aligning trench, wherein the insulation depositing step includes depositing the insulation without removing the coating (see column 14, lines 12-20).

In re claim, 11, Zhang et al. teaches that wherein the height difference between the upper surface of the insulation deposited in the mask aligning trench and the upper surface located lower than the upper surface of the semiconductor substrate is adjustable by said etching the insulation deposited in the mask aligning trench (see column 2, lines 35-50, column 4, lines 30-50 and column 1, lines 28-50).

In re claim 12, as best as understood by examiner, Kuroi et al. disclose the method of patterning a conductive film on the semiconductor substrate, wherein the height of the step at the time of removing the film is adjusted to a predetermined height that is equal to a depth etched during said patterning of the conductive film (see Figure 17).

In re claim 7, Kuroi et al. disclose the method of manufacturing a semiconductor device, comprising;

forming an silicon oxide film (3) on an upper surface of a semiconductor substrate;

forming a silicon nitride film (4) on the silicon oxide film;

partially removing the silicon nitride film and the oxide film (see column 14, lines 12-20);

forming an element partitioning trench (10C) and a mask aligning trench (10A) by etching the semiconductor substrate using a residue of the silicon nitride and silicon oxide films as a mask, wherein the element partitioning trench and the mask aligning trench have substantially the same depths (see column 14, lines 12-20);

simultaneously depositing a first layer of insulation and a second layer of insulation (2A, 2C) in the element partitioning trench and in the mask aligning trench, respectively, by a CVD process, wherein no other insulation layer has been deposited by a plasma process in the trenches prior to the insulation being deposited;

coating the first insulation with a protective mask (51) to fully cover the element partitioning trench (see Figure 4);

etching the second insulation while the first insulation is covered by the protective mask (See Figures 4, 5 and column 14, lines 37-41);

removing the protective mask (See Figure 5 and column 14, lines 49-50);

flattening an upper surface of the semiconductor device (see column 14, lines 42-54); and

selectively removing the silicon nitride film and the silicon oxide film so that a second step is formed between the upper surface of the semiconductor substrate and an upper surface of the first insulation (see column 14, lines 49-63 and Figure 5). The examiner notes that the insulation is made planar with the silicon nitride film, and then the silicon nitride film and the silicon oxide film are removed, thus a step will be formed between the upper surface of the substrate and the upper surface of the insulation layer as shown in Figure 5 of Kuroi et al. Further, the examiner notes that Applicants' own admitted prior art discloses that a step will be formed in this manner (see specification, page 3, line 25 through page 4, line 30, and Figure 1f).

Kuroi et al. does not disclose the method of removing the insulation deposited in the mask aligning trench so that a step is formed between an upper surface the semiconductor substrate and an upper surface of the second insulation.

Zhang et al. discloses the method wherein the removing the insulation deposited in the mask aligning trench so that a step is formed between an upper surface the semiconductor substrate and an upper surface of the second insulation (see Figure 4B and column 2, lines 35-50). It would have been obvious to one of ordinary skill in the art at the time the invention was made to remove the insulation deposited in the mask aligning trench so that a step is formed between an upper surface the semiconductor substrate and an upper surface of the second insulation, because as Zhang et al. disclose the method ensures that the step distance is great enough for the alignment mark to be readable (see Zhang et al. column 2, lines 35-50).

Kuroi et al. does not disclose the method of depositing the insulation by performing a chemical vapor deposition process consisting of high density plasma chemical vapor deposition (HDPCVD). Krivokapic et al. discloses the method of forming an insulation layer (34) by a chemical vapor deposition process consisting of HDPCVD (see column 5, lines 49-65). It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the insulation layer of Kuroi et al. by the HDPCVD process of Krivokapic et al., since as Krivokapic et al. disclose, HPCVD is a self-planarizing process which allows for a reduction of CMP times required in the subsequent steps.

In re claim 8, Kuroi et al. further disclose the method wherein the first insulation and the second insulation are made of the same material (2, silicon oxide).

In re claim 13, Zhang et al. teach the method wherein the height of the first step is adjustable by etching the second insulation (see column 2, lines 35-50, column 4, lines 30-50 and column 1, lines 28-50).

In re claim 14, as best as understood by examiner, Kuroi et al. disclose the method of patterning a conductive film on the semiconductor substrate, wherein the height of the second step at the time of removing the film is adjusted to a predetermined height that is equal to a depth etched during said patterning of the conductive film (see Figure 17).

In re claim 9, Kuroi et al. disclose the method for manufacturing a semiconductor device, the method comprising:

forming a film on an upper surface of a semiconductor substrate (3, 4);

forming an element partitioning trench (10C) and a mask aligning trench (10A) in a semiconductor substrate (1);

simultaneously depositing an insulation (2) in the element partitioning trench and the mask aligning trench by a CVD process;

applying a protective mask (51) on the insulation deposited in the element partitioning trench to fully cover the element partitioning trench (see Figure 4)

etching the insulation deposited in the mask aligning trench to remove some of the insulation while the insulation deposited in the element partitioning trench is covered by the protective mask (see Figure 4 and column 14, lines 37-41);

removing the protective mask (51, see Figure 5, and column 14, lines 49-51);

flattening an upper surface of the semiconductor device (see column 14, lines 42-54); and selectively removing the film so that a step is formed between the upper surface of the semiconductor substrate and an upper surface of the insulation in the element portioning trench. The examiner notes that the insulation is made planar with the silicon nitride film, and then the silicon nitride film and the silicon oxide film are removed, thus a step will be formed between the upper surface of the substrate and the upper surface of the insulation layer as shown in Figure 5 of Kuroi et al. Further, the examiner notes that Applicants' own admitted prior art discloses that a step will be formed in this manner (see specification, page 3, line 25 through page 4, line 30, and Figure 1f).

Kuroi et al. does not disclose the method of removing the insulation deposited in the mask aligning trench has an upper surface located lower than the upper surface of the semiconductor substrate.

Zhang et al. discloses the method wherein the removing the insulation deposited in the mask aligning trench has an upper surface located lower than the upper surface of the semiconductor substrate (see Figure 4B and column 2, lines 35-50). It would have been obvious to one of ordinary skill in the art at the time the invention was made to remove the insulation deposited in the mask aligning trench has an upper surface

located lower than the upper surface of the semiconductor substrate, because as Zhang et al. disclose the method ensures that the step distance is great enough for the alignment mark to be readable (see Zhang et al. column 2, lines 35-50).

Kuroi et al. does not disclose the method of depositing the insulation by performing a chemical vapor deposition process consisting of high density plasma chemical vapor deposition (HDPCVD). Krivokapic et al. disclose the method of forming an insulation layer (34) by a chemical vapor deposition process consisting of HDPCVD (see column 5, lines 49-65). It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the insulation layer of Kuroi et al. by the HDPCVD process of Krivokapic et al., since as Krivokapic et al. disclose, HPCVD is a self-planarizing process which allows for a reduction of CMP times required in the subsequent steps.

In re claim, 15, Zhang et al. teaches that wherein the height difference between the upper surface of the insulation deposited in the mask aligning trench and the upper surface located lower than the upper surface of the semiconductor substrate is adjustable by said etching the insulation deposited in the mask aligning trench (see column 2, lines 35-50, column 4, lines 30-50 and column 1, lines 28-50)

In re claim 16, as best as understood by examiner, Kuroi et al. disclose the method of patterning a conductive film on the semiconductor substrate, wherein the height of the step at the time of removing the film is adjusted to a predetermined height

that is equal to a depth etched during said patterning of the conductive film (see Figure 17).

In re claim 10, Kuroi et al. disclose the method of manufacturing a semiconductor device, comprising;

forming an silicon oxide film (3) on an upper surface of a semiconductor substrate;

forming a silicon nitride film (4) on the silicon oxide film;

partially removing the silicon nitride film and the silicon oxide film (see column 4, lines 10-19);

forming an element partitioning trench (10C) and a mask aligning trench (10A) by etching the semiconductor substrate using a residue of the silicon nitride and silicon oxide films as a mask, wherein the element partitioning trench and the mask aligning trench have substantially the same depths (see column 14, lines 12-20);

simultaneously depositing a first layer of insulation and a second layer of insulation (2A, 2C) in the element partitioning trench and in the mask aligning trench, respectively, by a CVD process, the first layer of insulation and the second layer of insulation directly contacting the semiconductor substrate;

coating the first insulation with a protective mask (51) to fully cover the element partitioning trench (see Figure 4);

etching the second insulation while the first insulation is covered by the protective mask (See Figures 4, 5 and column 14, lines 37-41);

removing the protective mask (See Figure 5 and column 14, lines 49-50); and

selectively removing the silicon nitride film and the silicon oxide film so that a step is formed between the upper surface of the semiconductor substrate and an upper surface of the first insulation (see column 14, lines 49-63 and Figure 5). The examiner notes that the insulation is made planar with the silicon nitride film, and then the silicon nitride film and the silicon oxide film are removed, thus a step will be formed between the upper surface of the substrate and the upper surface of the insulation layer as shown in Figure 5 of Kuroi et al. Further, the examiner notes that Applicants' own admitted prior art discloses that a step will be formed in this manner (see specification, page 3, line 25 through page 4, line 30, and Figure 1f).

Kuroi et al. does not disclose the method of removing the insulation deposited in the mask aligning trench so that a step is formed between an upper surface the semiconductor substrate and an upper surface of the second insulation.

Zhang et al. discloses the method wherein the removing the insulation deposited in the mask aligning trench so that a step is formed between an upper surface the semiconductor substrate and an upper surface of the second insulation (see Figure 4B and column 2, lines 35-50). It would have been obvious to one of ordinary skill in the art at the time the invention was made to remove the insulation deposited in the mask aligning trench so that a step is formed between an upper surface the semiconductor substrate and an upper surface of the second insulation, because as Zhang et al.

disclose the method ensures that the step distance is great enough for the alignment mark to be readable (see Zhang et al. column 2, lines 35-50).

Kuroi et al. does not disclose the method of depositing the insulation by performing a chemical vapor deposition process consisting of high density plasma chemical vapor deposition (HDPCVD). Krivokapic et al. discloses the method of forming an insulation layer (34) by a chemical vapor deposition process consisting of HDPCVD (see column 5, lines 49-65). It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the insulation layer of Kuroi et al. by the HDPCVD process of Krivokapic et al., since as Krivokapic et al. disclose, HPCVD is a self-planarizing process which allows for a reduction of CMP times required in the subsequent steps.

In re claim 17, Zhang et al. teach the method wherein the height of the first step is adjustable by etching the second insulation (see column 2, lines 35-50, column 4, lines 30-50 and column 1, lines 28-50)

In re claim 18, as best as understood by examiner, Kuroi et al. disclose the method of patterning a conductive film on the semiconductor substrate, wherein the height of the step at the time of removing the film is adjusted to a predetermined height that is equal to a depth etched during said patterning of the conductive film (see Figure 17).

Claims 5 and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kuroi et al. (U.S. Patent No. 5,889,335), Zhang et al. (U.S. Patent No. 6,303,458), and Krivokapic et al. (U.S. Patent No. 6,087,208) in view of Schoenfeld (U.S. Patent No. 6,127,245).

In re claim 5, Kuroi et al., Zhang et al., and Krivokapic et al. disclose the method as claimed and rejected above including the steps of flattening by a chemical mechanical process, wherein the coating functions as a stopper, but do not disclose that the method of flattening is performed rotary grinding. Schoenfeld discloses the method of utilizing a rotary grinder in CMP process (see column 5, lines 30-45). It would have been obvious to one of ordinary skill in the art at the time the invention was made to use a rotary grinding disc in the CMP process of the combined Kuroi et al. and Krivokapic et al. in order to create a uniform flat surface that allows for ease of formation of subsequently formed devices.

In re claim 6, Kuroi et al. disclose the method wherein the semiconductor substrate is a silicon substrate (1) the insulation is formed from silicon oxide (2), the coating is formed from silicon nitride (4); the method further comprising the step of forming a silicon oxide film (3) on the semiconductor substrate prior to the formation of the element partitioning trench and the mask aligning trench, wherein the coating is formed on the silicon oxide film (see Figure 2-3).

Response to Arguments

Applicant's arguments with respect to claims 3-18 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Wolf et al. (Silicon Processing for the VLSI Era, Volume 1-Process Technology, 1986, Lattice Press, page 1) discloses the advantages to silicon substrates and silicon oxide.

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jennifer M. Kennedy whose telephone number is (571) 272-1672. The examiner can normally be reached on Mon.-Fri. 9:30-6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael S. Lebentritt can be reached on (571) 272-1873. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jennifer M. Kennedy
Primary Examiner
Art Unit 2812

jmk